



09-11-06

AF/IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Shidemantle et al. : Art Unit: 2859
Serial No.: 10/783,491 : Docket No. 650271-132
(MSI-YSI-1-US)
Filed: February 20, 2004 : Examiner: Mirellys Jagan
For: DIGITALLY MODIFIED RESISTIVE OUTPUT FOR A TEMPERATURE
SENSOR

MAILSTOP AF
Commissioner for Patents P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL ACTION

Dear Sir:

Response to the Final Official Action mailed November 9, 2005 in the above-identified patent application was assigned a shortened statutory period, set to expire May 9, 2006. A Notice of Appeal and Petition for Extension of Time were filed May 9, 2006. Accordingly, Applicants deem this Amendment and Response timely filed by September 9, 2006 with a two month extension of time. Should there be any additional fees due and owing, or being paid in excess of any required amount, with respect to this application, the Examiner is authorized to charge such fees or to credit such overpayment to deposit account no. 50-3208.

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Please enter the following amendments and remarks:

CERTIFICATE OF MAILING UNDER 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail on August 29, 2006 in an envelope addressed to: Mailstop AF; Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Abby Melcher
Signature

Abby Melcher
Name

AMENDMENT TO THE CLAIMS

In the Claims:

Please amend the Claims as follows and without prejudice. This listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1-7. (Cancelled)

8. (Currently Amended) An interface for a monitor and a temperature probe including a temperature sensor comprising:

a logic circuit for determining a modified resistive output for the temperature sensor and

a means for providing the modified resistive output, wherein the means for providing the modified resistive output is compatible with the monitor such that the monitor can display a temperature that corresponds to the modified resistive output from the temperature probe.

9. (Original) The interface of claim 8 wherein the logic circuit is programmed to execute a predictive or a correlative algorithm.

10. (Original) The interface of claim 9 wherein the logic circuit is a microprocessor.

11. (Original) The interface of claim 8 wherein the means for providing the modified resistive output is a potentiometer and the logic circuit sends a control signal to the potentiometer such that the potentiometer provides the modified resistive output.

12. (Original) The interface of claim 11 wherein the probe includes two potentiometers.

13. (Original) The interface of claim 8 wherein the means for providing the modified resistive output includes a FET.

14. (Original) The interface of claim 8 wherein the means for providing the modified resistive output includes a photocell and an LED.

15. (Cancelled)

16. (Currently Amended) A temperature probe comprising:

a temperature sensor having a resistive output,

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm, and

a FET for providing the modified resistive output in response to a signal from the processor,

wherein the algorithm is a predictive algorithm that converts the resistive output of the temperature sensor during a thermally unstable condition to a modified resistive output representative of a predicted temperature during a condition of thermal stability.

17. (Original) The temperature probe of claim 16 wherein the processor executes an algorithm to convert the resistive output of the temperature sensor to a modified resistive output that can be displayed by a monitor.

18. (Cancelled)

19. (Previously Presented) The temperature probe of claim 16 wherein the probe includes two FETs.

20-24. (Cancelled)

25. (Previously Presented) A method for digitally modifying the resistive output of a temperature sensor which comprises inputting the resistive output from the temperature sensor to a logic circuit, implementing a predictive or a correlative algorithm using the logic circuit to determine a modified resistive output, controlling a gate of a FET to adopt a setting corresponding to the modified resistive output, and outputting a resistance corresponding to the modified resistive output.

26. (Cancelled)

27. (Currently Amended) ~~The temperature probe of claim 5,~~ A temperature probe comprising:

a temperature sensor that provides a resistive output,

a logic circuit for determining a modified resistive output for the temperature sensor, and

a means for providing the modified resistive output including a FET,

wherein the logic circuit is a microprocessor programmed to execute a predictive or a correlative algorithm, and

wherein the microprocessor includes an output and the FET includes a gate, where the output of the microprocessor controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

28. (Previously Presented) The temperature probe of claim 27 wherein the microprocessor further includes:

a first input from a first amplifier, where the first amplifier measures a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the microprocessor calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

29. (Previously Presented) The interface of claim 13 wherein the interface includes two FETs.

30. (Currently Amended) ~~The interface of claim 13~~ An interface for a monitor and a temperature probe including a temperature sensor comprising:

a logic circuit for determining a modified resistive output for the temperature sensor and

a means for providing the modified resistive output, wherein the means for providing the modified resistive output includes a FET, and

wherein the logic circuit includes an output and the FET includes a gate, where the output of the logic circuit controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

31. (Previously Presented) The interface of claim 30 wherein the logic circuit further includes:

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the logic circuit calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

32. (Currently Amended) A temperature probe comprising:

a temperature sensor having a resistive output,

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm, and

a FET for providing the modified resistive output in response to a signal from the processor,

~~The temperature probe of claim 16~~ wherein the processor includes an output and the FET includes a gate, where the output of the processor controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

33. (Previously Presented) The temperature probe of claim 32 wherein the processor further includes:

a first input from a first amplifier, where the first amplifier measure a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the processor calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

34. (Previously Presented) The method of claim 25 further including measuring a FET voltage with a first amplifier, measuring a resistor voltage of a first resistor having a first resistance, calculating a FET current using the first resistance and the resistor

voltage, calculating a FET resistance using the FET voltage and the FET current, comparing the FET resistance to the modified resistive output and applying a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

TELEPHONE INTERVIEW

The undersigned thanks the Examiner for the courtesy of a telephone interview conducted on or about August 21, 2006.

STATUS OF CLAIMS

Claims 1-34 are pending.

Claims 1-3, 5, 8-10, 13, 16, 17 and 20-22 stand rejected by the Examiner.

Claims 4, 6, 7, 11, 12, 14, 19, 23, 24, 26 and 29 stand withdrawn.

Claims 15, 18, 27, 28 and 30-33 stand objected to.

Claims 25 and 34 stand allowed.

Claims 8, 16, 27, 30 and 32 have been amended, without prejudice herein.

Claims 1-7, 15, 18, 20-24 and 26 have been cancelled without prejudice herein.

Reconsideration and allowance of this application is respectfully requested.

CHANGE OF CORRESPONDENCE ADDRESS

Applicants previously submitted (on August 7, 2006) a new Power of Attorney and a change of correspondence address. Applicants respectfully request all correspondence regarding this application be addressed to the address associated with Customer Number 45,722.

Allowable Subject Matter

Applicants gratefully acknowledge that Claims 25 and 34 are allowed. Applicants further gratefully acknowledge that claims 15, 18, 27, 28 and 30, 31, 32 and 33 stand objected to, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Solely for purposes of expediting allowance of this application, Applicants have amended the present Claims as follows.

Claims 1-7 have been canceled without prejudice herein.

Objected to Claim 15 depended directly from independent Claim 8. Independent Claim 8 has been amended to include the subject matter and limitations of dependent Claim 15, which claim was indicated as allowable if rewritten in independent form. Amended Claim 8 now contains the subject matter of dependent Claim 15, and is in condition for allowance. Claim 15 has been canceled without prejudice. Claims 9-14 and 29 depend ultimately from independent Claim 8. While Claims 11, 12, 14 and 29 were withdrawn as directed to a non-elected species, as amended Claim 8 is an allowable generic claim, Claims 11, 12 and 14 are now allowable. Allowance of Claims 9-14 is respectfully requested.

Objected to Claim 18 depended directly from independent Claim 16. Independent Claim 16 has been amended to include the subject matter of dependent Claim 18, which claim was indicated as allowable if rewritten in independent form. Amended Claim 16 now contains the subject matter of dependent Claim 18, and is in condition for allowance. Claim 18 has been cancelled without prejudice. Claims 17 and 19 depend ultimately from independent Claim 16. While Claim 19 was withdrawn as directed to a non-elected species, as Claim 16 is an allowable generic claim, Claim 19 is now allowable. Allowance of Claims 16, 17 and 19 is respectfully requested.

Claims 20-24 and 26 have been cancelled without prejudice.

Claims 25 and 34 stand allowed.

Claim 27 stands objected to, but is indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Claim 27 has been amended to be independent in form, including the all of the limitations of now canceled claims 1, 2, 3 and 5. Claim 28 depends from Claim 27. Allowance of amended Claim 27 and dependent Claim 28 is respectfully requested.

Claim 30 stands objected to, but is indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Claim 30 has been amended to be independent in form, to include the

limitations of previous Claim 13 and Claim 8, from which Claim 30 depended. Allowance of amended Claim 30 is respectfully requested. Claim 31 depends from amended Claim 30 and is likewise in condition for allowance, early notification of which is respectfully requested.

Claim 32 stands objected to, but is indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 32 depended directly from previous Claim 16. In response, Claim 32 has been amended to be independent in form, and to include all of the limitations of previous Claim 16. Allowance of amended Claim 32 is respectfully requested. Claim 33 depends from amended Claim 32 and is likewise in condition for allowance, early notification of which is respectfully requested.

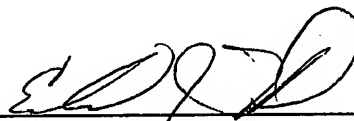
In view of the foregoing, Applicants submit that all of claims 8-14, 16, 17, 19, 25 and 27-34 presently appearing in the application are in condition for allowance. Such allowance is respectfully solicited.

CONCLUSION

Accordingly, Applicant believes he has addressed all outstanding grounds raised in the outstanding Office action, and respectfully submits the present case is in condition for allowance, early notification of which is earnestly solicited.

Should there be any questions or outstanding matters, the Examiner is cordially invited and requested to contact Applicant's undersigned attorney at his number listed below.

Respectfully submitted,



Edward J. Howard
Reg. No. 42,670
Plevy, Howard & Darcy, P.C.
P.O. Box 226
Fort Washington, PA 19034
(215) 542-5824
(215) 542-5825 (fax)

Dated: August 29, 2006

**COMBINED AMENDMENT & PETITION FOR EXTENSION OF
TIME UNDER 37 CFR 1.136(a) (Large Entity)**

Docket No.
650271-132

In Re Application Of: **Shiomi et al.**

Application No.
10/783,491

Filing Date
2/20/2004

Examiner
Mirellys Jagan

Customer No.
45,722

Group Art Unit
2859

Confirmation No.
2161

Invention: **DIGITALLY MODIFIED RESISTIVE OUTPUT FOR A TEMPERATURE SENSOR**

COMMISSIONER FOR PATENTS:

This is a combined amendment and petition under the provisions of 37 CFR 1.136(a) to extend the period for filing an Appeal Brief based on the Notice of Appeal filed May 9, 2006.

The requested extension is as follows (check time period desired):

☐ One month ☒ Two months ☐ Three months ☐ Four months ☐ Five months

from: July 9, 2006 until: September 9, 2006
Date Date

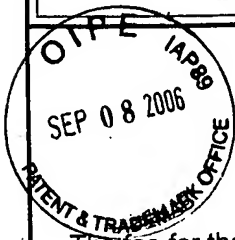
The fee for the amendment and extension of time has been calculated as shown below:

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	19 -	34 =	0	x \$50.00	\$0.00
INDEP. CLAIMS	6 -	5 =	1	x \$200.00	\$200.00
FEE FOR AMENDMENT					\$200.00
FEE FOR EXTENSION OF TIME					\$450.00
TOTAL FEE FOR AMENDMENT AND EXTENSION OF TIME					\$650.00

**COMBINED AMENDMENT & PETITION FOR EXTENSION OF
TIME UNDER 37 CFR 1.136(a) (Large Entity)**

Docket No.
650271-132



The fee for the amendment and extension of time is to be paid as follows:

- ☒ A check in the amount of **\$650.00** for the amendment and extension of time is enclosed.
- ☐ Please charge Deposit Account No. _____ in the amount of _____
- ☒ The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. **50-3208**
- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☐ Any patent application processing fees under 37 CFR 1.17.
- ☒ If an additional extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to Deposit Account No. **50-3208**
- ☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.


Signature

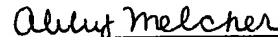
Edward J. Howard
Reg. No. 42,670
Plevy, Howard & Darcy, PC
P.O. Box 226
Fort Washington, PA 19034
(215) 542-5824

Dated: August 29, 2006

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

August 29, 2006

(Date)



Signature of Person Mailing Correspondence

Abby Melcher

Typed or Printed Name of Person Mailing Correspondence

CC: